Amendments to the Claims:

A clean version of the entire set of pending claims, including amendments to the claims, is submitted herewith per 37 CFR 1.121(c)(3). This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-15. (Canceled).

16. (Previously Presented) A TFT comprising a substrate a gate overlying the substrate and having side edges inclined towards one another, a channel region overlying the gate and source and drain regions overlying said side edges respectively, wherein the gate has been formed on the substrate by an etching process that involved formation of a tip in an apex region between the side edges of a radius of a few nanometres.

17. (Currently Amended) A TFT according to claim 16 wherein the tip ~~(13)~~ was removed before the channel region was applied.

18. (Previously Presented) A TFT according to claim 16 wherein the gate is overlaid by a layer of insulating material, the channel region overlies the insulating material, a layer of doped semiconductor material overlies the channel region, and a layer of conductive material from which said source and drain regions have been formed, overlies the doped semiconductor material.

19. (Currently Amended) A TFT according to claim 16 wherein the channel region ~~(6)~~ comprises intrinsic amorphous silicon.

20. (Currently Amended) A TFT according to claim 18 wherein the insulating layer comprises ~~(5)~~ silicon nitride.

21. (Original) A TFT according to claim 18 wherein the doped semiconductor material (7) comprises n doped silicon.

22. (New) The TFT of claim 16, wherein the channel region has a length of 20-40 nanometers.

23. (New) The TFT of claim 22, further comprising an insulating material disposed between the gate and the substrate.

24. (New) A thin film transistor (TFT), comprising:

a gate disposed on a substrate, the gate having side edges inclined towards one another to reach a tip having a radius of a few nanometers,

a gate insulating later disposed on the gate;

a channel region disposed on the gate insulating layer;

a source electrode overlying a first side edge of the gate, and

a drain electrode overlying a second side edge of the gate.

25. (New) The TFT of claim 24, further comprising a layer of doped semiconductor material overlying the channel region.

26. (New) The TFT of claim 24, wherein the channel region has a length of 20-40 nanometers.

27. (New) The TFT of claim 24, further comprising an insulating material disposed between the gate and the substrate.

28. (New) The TFT of claim 24, wherein the channel region comprises intrinsic amorphous silicon.